

MEMS HIGH FREQUENCY OSCILLATOR

■ FEATURES

- Output frequency from 80M~220MHz
- Low phase jitter : 0.5ps (12KHz to 20MHz)
- LVC MOS/HCMOS outputs
- Industry-standard packages: 2.5x2.0, 3.2x2.5, 5.0x3.2, 7.0x5.0
- RoHS and REACH compliant

■ APPLICATIONS

- 10G Ethernet, SONET, Networking
- SATA, SAS, Storage, PCI-Express
- Telecom, Industrial Control



■ ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	80	–	220	MHz	
Frequency Stability and Aging						
Frequency Stability	F_stab	-10	–	+10	ppm	Inclusive of initial tolerance at 25°C, 1 st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load.
		-20	–	+20	ppm	
		-25	–	+25	ppm	
		-50	–	+50	ppm	
First Year Aging	F_aging	-1.5	-	+1.5	Ppm	@ 25°C
10 Year Aging		-5	-	+5	ppm	
Operating Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage and Current Consumption						
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	34	36	mA	No load condition, f = 100 MHz, Vdd = 2.5V, 2.8V, 3.3V
		–	30	33	mA	No load condition, f = 100 MHz, Vdd = 1.8V
OE Disable Current	I_OD	–	–	31	mA	Vdd = 2.5V, 2.8V, 3.3V, OE = GND, Output is weakly pulled down
		–	–	30	mA	Vdd = 1.8V, OE = GND, Output is weakly pulled down
Standby Current	I_std	–	-	70	μA	$\overline{ST}$ = GND, Vdd = 2.5V, 2.8V, 3.3V, Output is weakly pulled down
		–	-	10	μA	$\overline{ST}$ = GND, Vdd = 1.8V, Output is weakly pulled down

LVC MOS Output Characteristics

Duty Cycle	DC	45	–	55	%	All Vdds. f ≤ 165MHz
		40	–	60	%	All Vdds. f > 165MHz
Rise/Fall Time	Tr, Tf	–	1.2	2	ns	15pF load, 10% - 90%
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -6 mA, IOL = 6 mA, (Vdd = 3.3V, 2.8V, 2.5V) IOH = -3 mA, IOL = 3 mA, (Vdd = 1.8V)
Output Low Voltage	VOL	–	–	10%	Vdd	

Input Characteristics

Input High Voltage	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Low Voltage	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z_in		100	250	kΩ	Pin 1, OE logic high or logic low, or $\overline{ST}$ logic high
		2	–	–	MΩ	Pin 1, $\overline{ST}$ logic low

Startup and Resume Timing

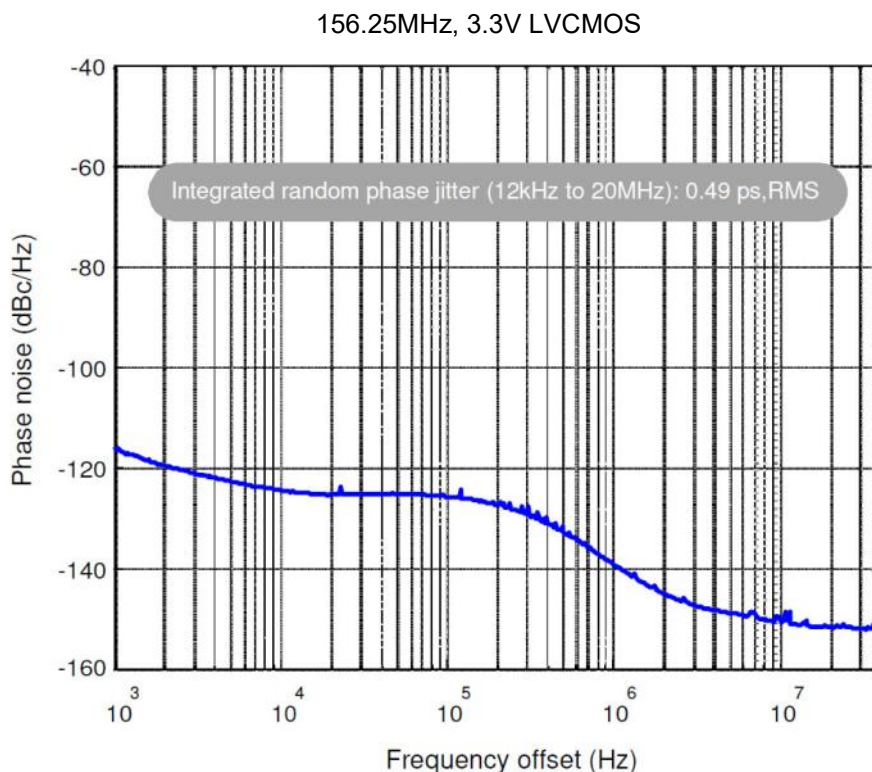
Startup Time	T_start	–	7	10	ms	Measured from the time Vdd reaches its rated minimum value
Enable/Disable Time	T_oe	–	–	115	ns	f = 80 MHz. For other frequencies, T_oe = 100 ns + 3 cycles
Resume Time	T_resume	–	–	10	ms	Measured from the time $\overline{ST}$ pin crosses 50% threshold

Jitter

RMS Period Jitter	T_jitt	–	1.5	2	ps	f = 156.25MHz, Vdd = 2.5V, 2.8V, or 3.3V
		–	2	3	ps	f = 156.25MHz, Vdd = 1.8V
RMS Phase Jitter (random)	T_phj	–	0.5	1	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz

- All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated.
- Typical values are at 25°C and nominal supply voltage.

■ TYPICAL PHASE NOISE



■ ABSOLUTE MAXIMUM LIMITS

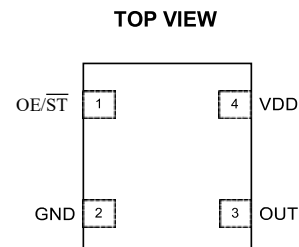
Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	—	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	—	260	°C
Junction Temperature	—	150	°C

■ PIN DESCRIPTION

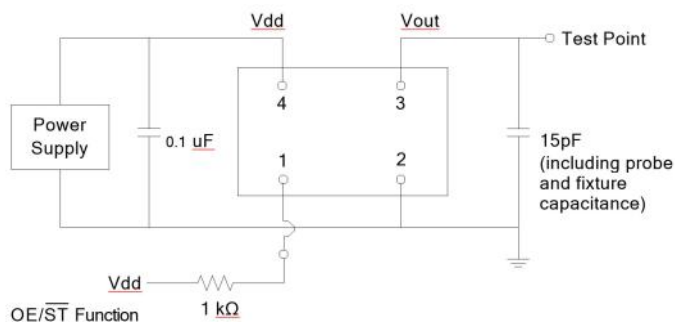
Pin	Symbol		Function
1	OE/ $\overline{\text{ST}}$	Output Enable	H or OPEN ^[1] : specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H or OPEN ^[1] : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I _{std} .
2	GND	Power	Electrical ground ^[2]
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage ^[2]

■ PIN ASSIGNMENTS

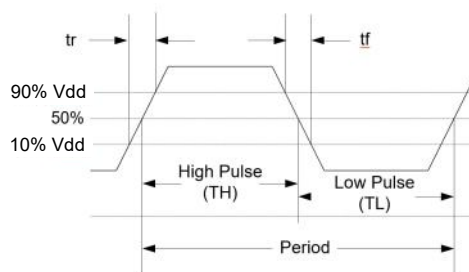


1. A pull-up resistor of <10 k Ω between OE/ ST pin and Vdd is recommended in high noise environment.
2. A capacitor of value 0.1 μF or higher between Vdd and GND is required

■ TEST CIRCUIT



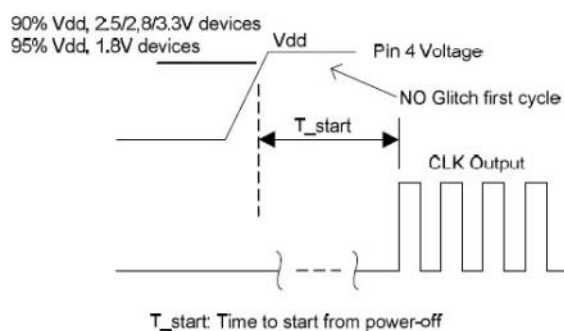
■ WAVEFORM



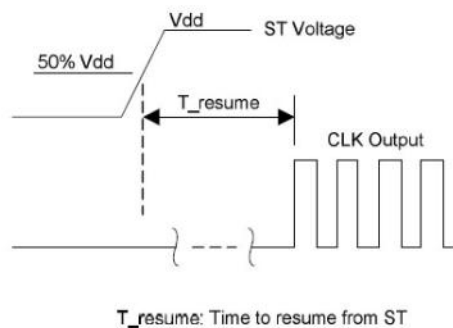
Duty Cycle is computed as Duty Cycle = TH/Period.

■ TIMING DIAGRAMS

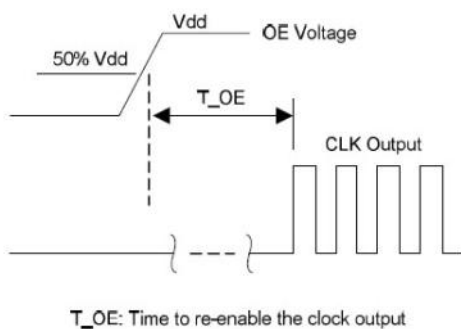
Startup Timing (OE / $\overline{ST}$ Mode)



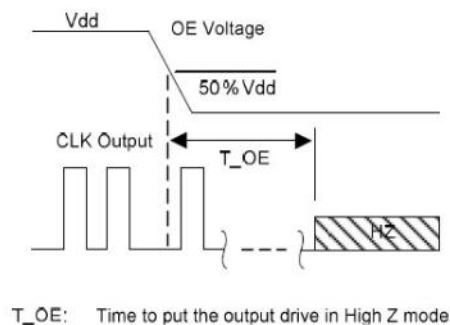
Standby Resume Timing ($\overline{ST}$ Mode Only)



OE Enable Timing (OE Mode Only)

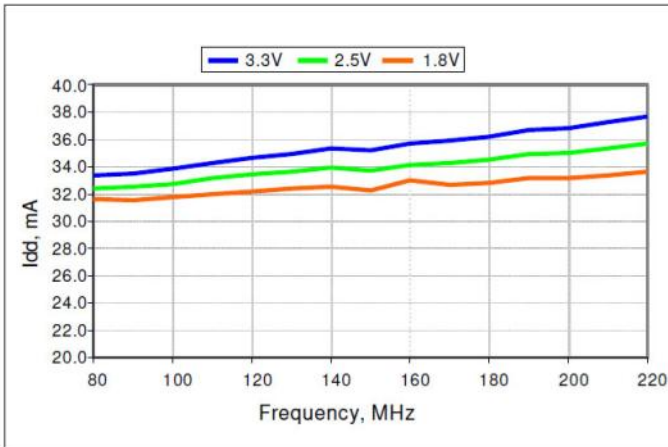


OE Disable Timing (OE Mode Only)

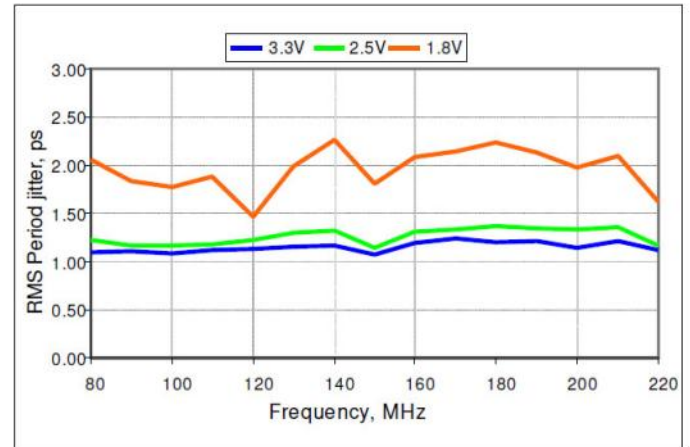


■ PERFORMANCE PLOTS

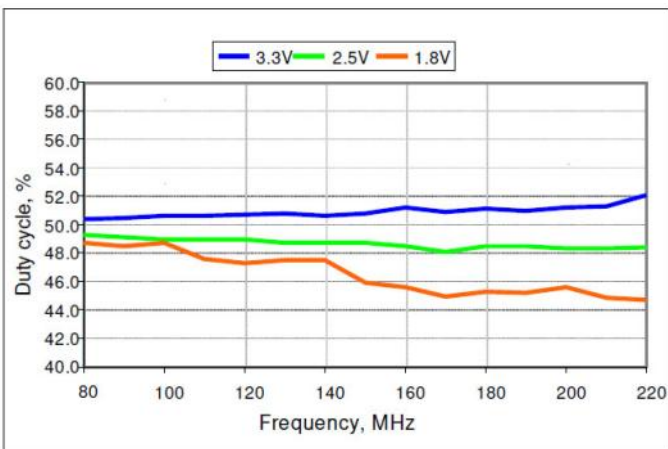
All plots are measured with 15 pF load at room temperature, unless otherwise stated.



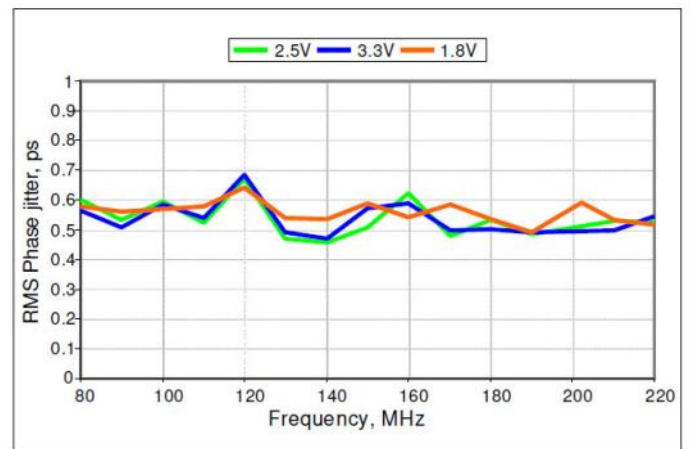
Idd vs Frequency



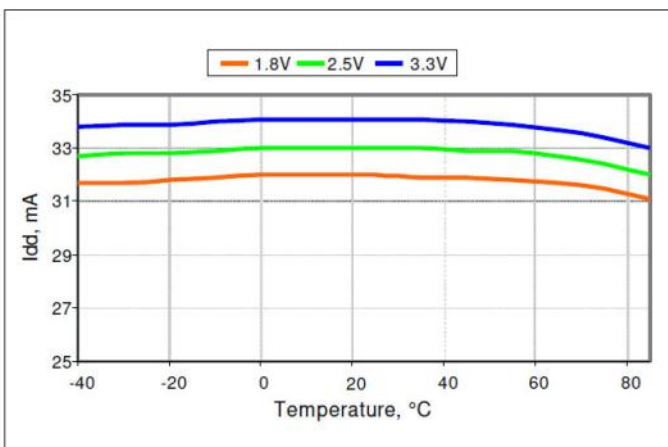
RMS Period Jitter vs Frequency



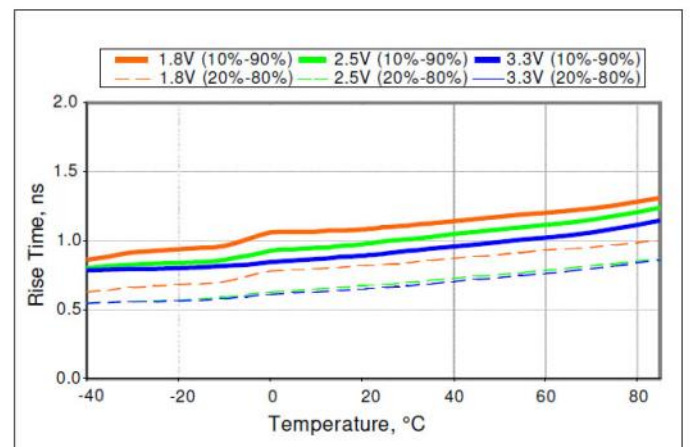
Duty Cycle vs Frequency



RMS Phase Jitter vs Frequency



Idd vs Temperature, 100MHz Output



Rise Time vs Temperature 100MHz Output

■ OUTPUT DRIVE STRENGTH—RISE / FALL TIME OPTIONS

Rise/Fall Time Typ (ns) Vdd = 1.8V					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	12.45	17.68	19.48	46.21	57.82
A	6.50	10.27	16.21	23.92	30.73
R	4.38	7.05	11.61	16.17	20.83
B	3.27	5.30	8.89	12.18	15.75
S	2.62	4.25	7.20	9.81	12.65
D	2.19	3.52	6.00	8.31	10.59
T	1.76	3.01	5.14	7.10	9.15
E	1.59	2.59	4.49	6.25	7.98
U	1.49	2.28	3.96	5.55	7.15
F	1.22	2.10	3.57	5.00	6.46
W	1.07	1.88	3.23	4.50	5.87
G	1.01	1.64	2.95	4.12	5.40
X	0.96	1.50	2.74	3.80	4.98
K	0.92	1.41	2.56	3.52	4.64
Y	0.88	1.34	2.39	3.25	4.32
Q	0.86	1.29	2.24	3.04	4.06
Z or "-": Default	0.82	1.24	2.07	2.89	3.82
M	0.77	1.20	1.94	2.72	3.61
N	0.66	1.15	1.84	2.58	3.41
P	0.51	1.09	1.76	2.45	3.24

Rise/Fall Time Typ (ns) Vdd = 2.5V					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	8.68	13.59	18.36	32.70	42.06
A	4.42	7.18	11.93	16.60	21.38
R	2.93	4.78	8.15	11.19	14.59
B	2.21	3.57	6.19	8.55	11.04
S	1.67	2.87	4.94	6.85	8.80
D	1.50	2.33	4.11	5.68	7.33
T	1.06	2.04	3.50	4.84	6.26
E	0.98	1.69	3.03	4.20	5.51
U	0.93	1.48	2.69	3.73	4.92
F	0.90	1.37	2.44	3.34	4.42
W	0.87	1.29	2.21	3.04	4.02
G or "-": Default	0.67	1.20	2.00	2.79	3.69
X	0.44	1.10	1.86	2.56	3.43
K	0.38	0.99	1.76	2.37	3.18
Y	0.36	0.83	1.66	2.20	2.98
Q	0.34	0.71	1.58	2.07	2.80
Z	0.33	0.65	1.51	1.95	2.65
M	0.32	0.62	1.44	1.85	2.50
N	0.31	0.59	1.37	1.77	2.39
P	0.30	0.57	1.29	1.70	2.28

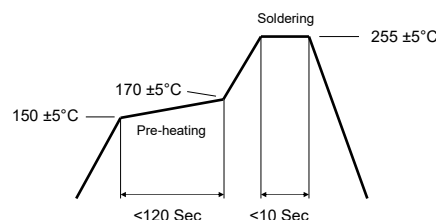
Rise/Fall Time Typ (ns) Vdd = 2.8V					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.93	12.69	17.94	30.10	38.89
A	4.06	6.66	11.04	15.31	19.80
R	2.68	4.40	7.53	10.29	13.37
B	2.00	3.25	5.66	7.84	10.11
S	1.59	2.57	4.54	6.27	8.07
D	1.19	2.14	3.76	5.21	6.72
T	1.00	1.79	3.20	4.43	5.77
E	0.94	1.51	2.78	3.84	5.06
U	0.90	1.38	2.48	3.40	4.50
F	0.87	1.29	2.21	3.03	4.05
W	0.62	1.19	1.99	2.76	3.68
G or "-": Default	0.41	1.08	1.84	2.52	3.36
X	0.37	0.96	1.72	2.33	3.15
K	0.35	0.78	1.63	2.15	2.92
Y	0.33	0.67	1.54	2.00	2.75
Q	0.32	0.63	1.46	1.89	2.57
Z	0.31	0.60	1.39	1.80	2.43
M	0.30	0.57	1.31	1.72	2.30
N	0.30	0.56	1.22	1.63	2.22
P	0.29	0.54	1.13	1.55	2.13

Rise/Fall Time Typ (ns) Vdd = 3.3V					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.18	11.59	17.24	27.57	35.57
A	3.61	6.02	10.19	13.98	18.10
R	2.31	3.95	6.88	9.42	12.24
B	1.65	2.92	5.12	7.10	9.17
S	1.43	2.26	4.09	5.66	7.34
D	1.01	1.91	3.38	4.69	6.14
T	0.94	1.51	2.86	3.97	5.25
E	0.90	1.36	2.50	3.46	4.58
U	0.86	1.25	2.21	3.03	4.07
F or "-": Default	0.48	1.15	1.95	2.72	3.65
W	0.38	1.04	1.77	2.47	3.31
G	0.36	0.87	1.66	2.23	3.03
X	0.34	0.70	1.56	2.04	2.80
K	0.33	0.63	1.48	1.89	2.61
Y	0.32	0.60	1.40	1.79	2.43
Q	0.32	0.58	1.31	1.69	2.28
Z	0.30	0.56	1.22	1.62	2.17
M	0.30	0.55	1.12	1.54	2.07
N	0.30	0.54	1.02	1.47	1.97
P	0.29	0.52	0.95	1.41	1.90

■ ENVIRONMENTAL COMPLIANCE

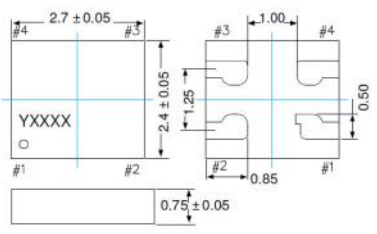
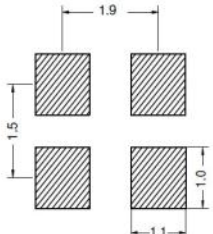
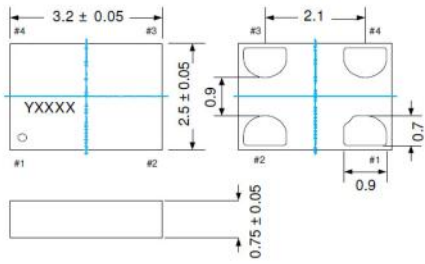
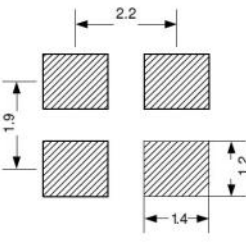
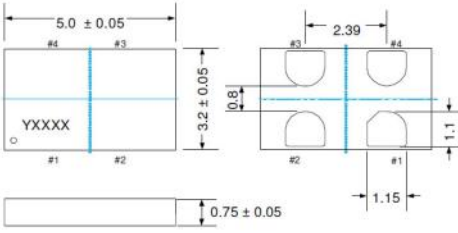
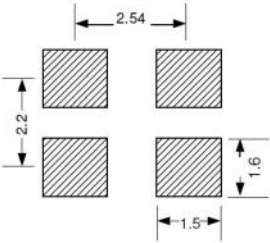
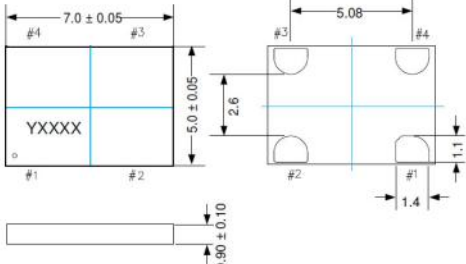
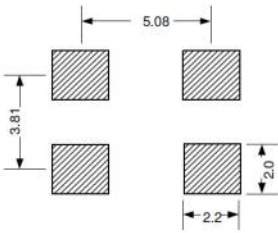
Parameter	Condition / Test Method
Mechanical Shock	MIL-STD-883F, Method2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method2003
Moisture Sensitivity Level	MSL1 @ 260°C

■ REFLOW PROFILE



Note: Consult factory for detail

■ PACKAGE OPTIONS / LAND PATTERN (Unit:mm)

PACKAGE 22	2.7 x 2.4 x 0.75 mm (100% compatible with 2.5 x 2.0 mm footprint) 	
PACKAGE 32	3.2 x 2.5 x 0.75 mm 	
PACKAGE 53	5.0 x 3.2 x 0.75 mm 	
PACKAGE 75	7.0 x 5.0 x 0.90 mm 	

MARKING

Y = FACTORY CODE
 XXXX = LOT CODE
 O = PIN 1 LOCATION

A capacitor of value 0.1 μ F or higher between Vdd and GND is required.

■ PART NUMBERING GUIDE

