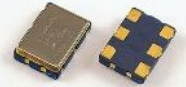


CERAMIC SMD LVDS/LVPECL OUTPUT OSCILLATOR (7.0 x 5.0 x 1.6mm)
FEATURES:

- LOW CURRENT
- ULTRA LOW <0.2ps RMS JITTER PERFORMANCE
- LOW COST

APPLICATIONS:

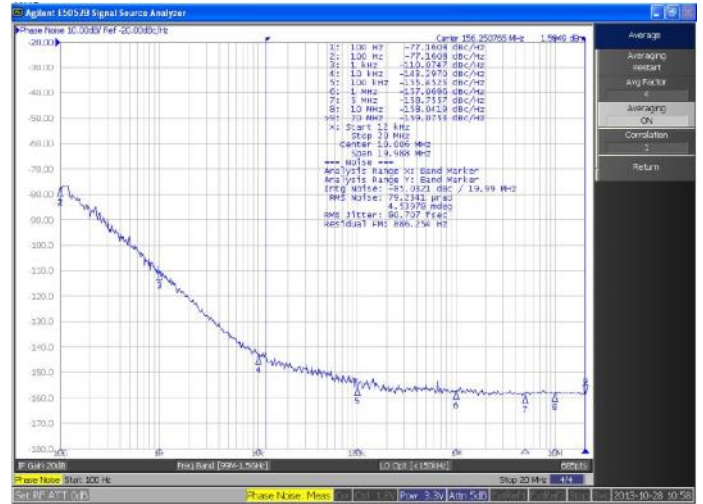
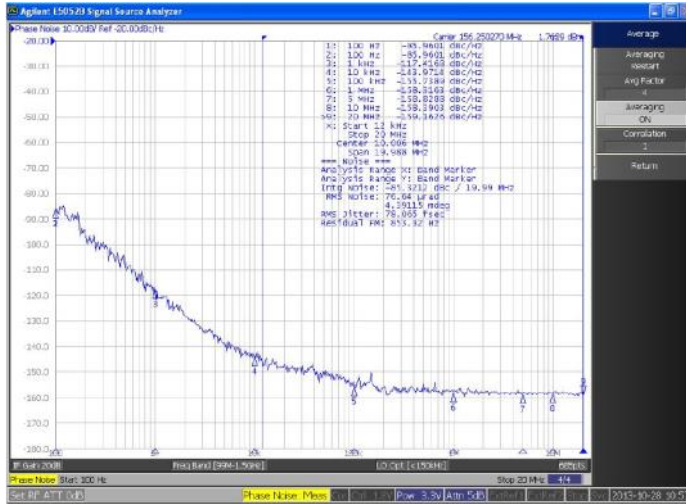
- 10GbE / 40GbE Ethernet Switches and Routers
- 100GbE Ethernet Switches and Routers
- Synchronous Ethernet


■ SPECIFICATION

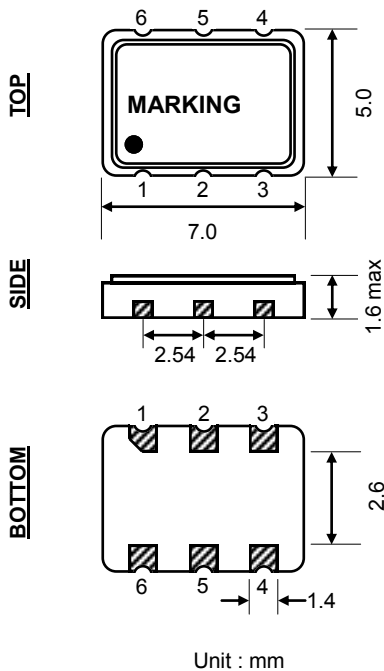
PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTE	
FREQUENCY RANGE		25		200	MHz		
FREQUENCY STABILITY		±10*	±50	±100	ppm	* Selected operating temp. only	
OPERATING TEMPERATURE RANGE		-40		85	°C	See P/N guide for other options	
STORAGE TEMPERATURE RANGE		-55		125	°C		
SUPPLY VOLTAGE ±10%		V _{DD} = 2.5V _{DC}	2.375	2.500	2.625	V	See P/N guide for other options
		V _{DD} = 3.3V _{DC}	2.970	3.300	3.630	V	
SUPPLY CURRENT				80	mA	(V _{DD} = 2.5V _{DC} , 3.3V _{DC})	
OUTPUT	LOAD	LVDS		100	Ω	Output - Complimentary Output	
		LVPECL		50	Ω	into V _{DD} - 2V _{DC}	
	LEVEL	LVDS (V _{OH})		1.4	1.6	V	
		LVDS (V _{OL})	0.9	1.1		V	
		LVPECL (V _{OH})	V _{DD} - 1.025V			V	
		LVPECL (V _{OL})			V _{DD} - 1.62V	V	
	PEAK TO PEAK	LVPECL	600	800		mV	
	DIFFERENTIAL OUTPUT VOLTAGE	LVDS	0.247	0.350	0.454	V	
	OFFSET VOLTAGE	LVDS	1.125	1.25	1.375	V	
	SYMMETRY (DUTY CYCLE)		40		60	%	
	RISE AND FALL TIME (Tr/Tf)			250	1000	pS	@ 20% / 80%
	START-UP TIME			5	10	mS	
STAND-BY VOLTAGE		ENABLE (V _{IH})	0.7 x V _{DD}			V _{DD}	
		DISABLE (V _{IL})			0.3 x V _{DD}	V _{DD}	
ENABLE DELAY TIME				100	nS		
DISABLE DELAY TIME				100	nS		
AGING		per 1year			±3.0	ppm	@ 25°C ±3°C
		per 10years			±5.0	ppm	
PHASE JITTER RMS		LVDS			0.6	pS	@ 12kHz ~ 20MHz
		LVPECL			0.2	pS	@ 12kHz ~ 20MHz
					0.1	pS	@ 10kHz ~ 1MHz
JITTER pk-pk		LVPECL			35	pS	@ 100,000 random periods

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■ PHASE NOISE

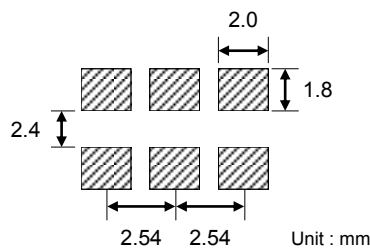


■ PACKAGE DIMENSIONS

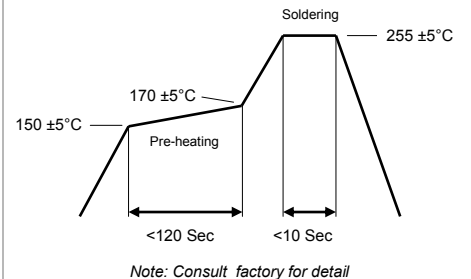


Pin Configuration	
1	En/Dis or N.C.
2	N.C
3	GND
4	Output
5	C - output
6	V _{DD}

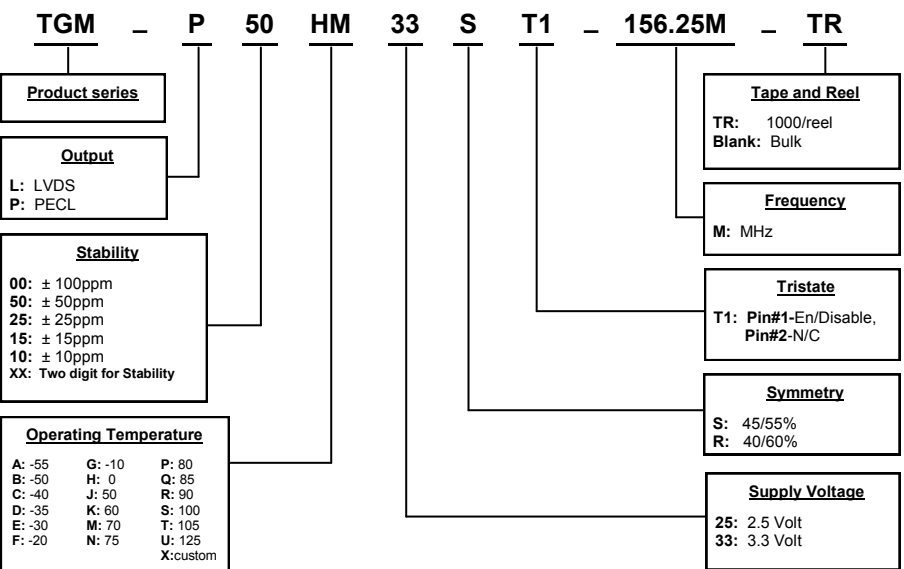
■ SOLDER PATTERN



■ REFLOW PROFILE



■ PART NUMBERING GUIDE



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